Applicants respectfully request reconsideration of the claims and the rejections.

Claims 1 and 11 claim a subsystem essential data processing functionality largely residing in reprogrammable logic device components. As defined in the specification: "as used herein, the essential functionality comprises the function to be performed by the subsystem, such as generating a transmit waveform for a transmit beamformer subsystem or scan converting data from an acoustic grid to a display format for a scan converter. In one embodiment, the essential functionality largely (i.e. at least 40% of the processing or signal path) resides in one or more re-programmable logic devices." (page 14, lines 7-12).

Wright et al. disclose a flexible beamformer system (col. 4, lines 38-41). The beamformer is programmable, such as downloading filter coefficients and decimation factors (col. 7, lines 38-49). However, Wright et al. do not disclose reprogrammable logic device components for implementing the programmable beamformer system. As defined in the specification: "as used herein, a re-programmable logic device comprises a plurality of logic elements the gate interconnections of which can be modified by an external data set loaded under software control by a processor residing in the system. Such re-programmable logic devices include field programmable gate arrays (FPGA), flash PROM FPGA, static random access memory FPGA (SRAM FPGA) , anti-fuse programmable logic devices, complex-programmable logic devices (C-PLD), electrically erasable PLD devices and other re-programmable PLD devices." (page 13, line 27-page 14, line 2). Wright et al. do not disclose a subsystem essential data processing functionality largely residing in reprogrammable logic device components.

Cole et al. disclose using a field programmable gate array for implementing a multiplexer scheme (col. 12, lines 48-52). Various channels are switched during transmit and receive (col. 12, lines 30-48). However, the field programmable gate arrays of Cole et al. are not used for data processing, only data routing. Cole et al. do not disclose a subsystem essential data processing functionality largely residing in reprogrammable logic device components.[1]

[1] See the previously submitted declarations of John Williams regarding use of FPGA's in Acuson's Sequoia ultrasound system. The Wright et al. and Cole et al. patents also disclose aspects of the Sequoia ultrasound system.

PAGE 2/8 * RCVD AT 4/19/2005 7:41:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):02-56

The remaining references using an FPGA cited by the Examiner do not disclose a subsystem essential data processing functionality largely residing in reprogrammable logic device components as claimed by claims 1 and 11. Doi et al. disclose an FPGA as one possible of many components on a motherboard (col. 5, lines 40-46). The Examiner lists various devices as stated equivalents, but Doi et al. do not discuss all the listed possible devices as equivalents. Further, Doi et al. do not disclose how any FPGA is used.

Muzilla et al. disclose converting flow estimates to 8 bit and 4-bit outputs and applying thresholding with a output logic block (col. 6, lines 17-25). The output logic block includes a field programmable gate array which selects parameters to be displayed (col. 11, lines 13-19). The output logic block also performs median filtering of M-mode data (col. 11, lines 25-27). The output logic block is a small part of the color processing flow system (col. 4, lines 21-22; Figure 3). Muzilla et al. do not disclose using FPGA devices for the essential data processing functionality of a subsystem.

Deitrich et al. use an FPGA for controlling interpolation by other components (col. 4, lines 56-60 and col. 5, lines 42-49). Deitrich et al. do not suggest using FPGA devices for the essential data processing functionality of a subsystem.

Likewise, Snyder discloses using a FPGA as a logic controller (col. 5, lines 26-39). The logic controller maps the switching function of a multiplexer (col. 5, lines 50-53 and 61-65). Snyder does not disclose using FPGA devices for the essential data processing functionality of a subsystem.

Similarly, McMorrow et al. (U.S. Patent No. 5,235,985) disclose using an FPGA for multiplexing (col. 5, line 66-col. 6, line 1). McMorrow et al. do not suggest using FPGA devices for the essential data processing functionality of a subsystem.

The Examiner stated that the language "a subsystem essential data processing functionality largely residing in programmable logic devices" is subjective, and instead converts the language into meaning not able to operate without the function. Applicants respectfully submit that the language is not subjective and should not be interpreted as done by the Examiner. The language is defined in the specification. "As used herein, the essential functionality comprises the function to be performed by the subsystem, such as generating a transmit waveform for a transmit beamformer subsystem or scan converting data from an acoustic grid to a display format for a scan converter. In one embodiment, the essential functionality largely

PAGE 3/8 * RCVD AT 4/19/2005 7:41:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):02-56

(i.e. at least 40% of the processing or signal path) resides in one or more re-programmable logic devices." (page 14, lines 7-12). This definition and the use in the claims provide objective meaning. First, data processing function is implemented. Dietrich, Synder and McMarrow use re-programmable logic devices for control functions, not data processing functions. Doi et al. do not indicate how the re-programmable logic devices are used. Second, the data processing must reside largely (e.g. 40% of processing or signal path) within the re-programmable logic devices. Muzilla et al. use a re-programmable logic device for selecting data that is converted, thresholded, and filtered in an output logic block of a color processing flow system. There is no indication of a large amount of data processing by re-programmable logic device in Muzilla et al. Selection of parameters for display is also not an essential function of the color processing flow system, such as detecting flow and assigning color values.

Scheib et al. and Pflugrath et al. do not suggest using re-programmable logic devices for data processing in an ultrasound subsystem. Both references teach use of reprogrammable EEPROMs. EEPROMs are memory devices, not electronically reprogrammable logic devices. Re-programmable logic devices are defined in the specification as: "As used herein, a re-programmable logic device comprises a plurality of logic elements the gate interconnections of which can be modified by an external data set loaded under software control by a processor residing in the system. Such re-programmable logic devices include field programmable gate arrays (FPGA), flash PROM FPGA, static random access memory FPGA (SRAM FPGA) , anti-fuse programmable logic devices, complex-programmable logic devices (C-PLD), electrically erasable PLD devices and other re-programmable PLD devices." (page 13, line 27-page 14, line 2). EEPROMs store information, but do not provide reprogrammable logic devices.

Applicants respectfully submit that a person of ordinary skill in the art would not have provided a subsystem's essential data processing functionality largely residing in re-programmable logic devices based on Hall and Zellinga et al. Hall is for infra-red imaging visible objects and Zellinga et al. is MRI, not medical diagnostic ultrasound imaging. Applicants respectfully submit that there is no motivation to use re-programmable logic devices in medical diagnostic ultrasound as claimed. The Examiner alleges that two imaging examples show general progress into adopting re-programmable logic devices for core functions in imaging, thus resulting in use in ultrasound imaging. However, a mere two examples do not show general progress. Furthermore, the examples do not show use of re-programmable logic devices as

PAGE 4/8 * RCVD AT 4/19/2005 7:41:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):02-56

claimed even in non-ultrasound contexts. Hall uses re-programmable logic devices in two ways. First, re-programmable logic devices are used for control functions (col. 7, lines 2-6), not data processing. Second, re-programmable logic devices are used for a convolver that also has a correlator (col. 7, lines 11-18). The function of a convolver is basically correlation, so the EPLDs are not used for a core function. Zellenga et al. use re-programmable logic devices for control, not data processing (col. 10, lines 15-23). A control sequencer is shown in the cited figures 7-11 and 13 (col. 9, lines 63-68; col. 14, lines 45-58; col. 18, lines 60-63; col. 19, lines 48-54; col. 23, lines 16-17 and 29-32; and col. 24, lines 16-17and 42-44). Applicants submit that the cited references do not use re-programmable logic devices for essential data processing functions, and thus do not suggest progress of re-programmable logic devices into imaging data processing or ultrasound data processing. Even if Halls use of re-programmable logic devices in the convolver provides essential data processing function of a subsystem largely residing in an re-programmable logic device, a single example in a very different type of imaging would not have suggested a general progress of re-programmable logic devices into imaging, thus a person of ordinary skill in the art would not have used re-programmable logic devices in ultrasound imaging for essential data processing functions.

Dependent claims 2-10, 12-20, 48-49, 51-53 and 55 depend from independent claims 1 and 11, and are thus are allowable for at least the same reasons as discussed above. Further distinctions over the prior art are not provided herein for brevity but will be provided if requested by the Examiner.

As discussed below, none of the references cited by the Examiner disclose a reprogrammable logic device in a beamformer as claimed in claims 6 and 7.

Claims 21 and 26 claim a beamformer comprising at least one re-programmable logic device. None of the cited references disclose this limitation. As discussed above, Wright et al. do not disclose reprogrammable logic device components for implementing the programmable beamformer system. Cole et al., McMorrow, and Snyder use FPGAs for multiplexing, not as a beamformer. Hall uses re-programmable logic devices in a controller and a convolver. Zellinga et al. use re-programmable logic devices in a controller for a sequencer. The Examiner does not cite to a beamformer with at least one re-programmable logic device in any of the other listed references.

PAGE 5/8 * RCVD AT 4/19/2005 7:41:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):02-56

Dependent claims 22-25, 27-30, 56-57, 59-61 and 63 depend from independent claims 21 and 26, and are thus allowable for at least the same reasons discussed above. Further distinctions over the prior art are not provided herein for brevity but will be provided if requested by the Examiner.

Claims 31 and 34 claim a scan converter comprising at least one but less than three re-programmable logic devices. None of Wright et al., Cole et al., Doi et al., Muzilla, Deitrich et al., Snyder, McMorrow, Hall nor Zellinga et al. disclose a scan converter having one to three re-programmable logic devices. Wright et al. does not disclose reprogrammable logic device components for implementing a scan converter. Cole et al., McMorrow, and Snyder use FPGAs for multiplexing, not as a scan converter. Doi et al. disclose an ultrasound system that may have an FPGA and/or other devices, not a scan converter with a re-programmable logic device. Muzilla discloses an FPGA for selecting data, but does not suggest a scan converter having a re-programmable logic device. Zellinga et al. and Deitrich et al. use an FPGA or EPLD for control, not scan conversion. Hall use re-programmable logic devices for correlating frames of data together to predict displacement, not as a scan converter.

Dependent claims 32-33, 35-36, 65 and 67 depend from independent claims 31 and 34, and are thus allowable for at least the same reasons discussed above. Further distinctions over the prior art are not provided herein for brevity but will be provided if requested by the Examiner.

PAGE 6/8 * RCVD AT 4/19/2005 7:41:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):02-56

Applicants respectfully submit that all of the pending claims are in condition for allowance and seeks early allowance thereof. If for any reason, the Examiner is unable to allow the application in the next Office Action and believes that an interview would be helpful to resolve any remaining issues, he is respectfully requested to contact the undersigned attorney at (650) 943-7350 or Craig Summerfield at (312) 321-4726.

PLEASE MAIL CORRESPONDENCE TO:

Siemens Corporation
Customer No. 28524
Attn: Elsa Keller, Legal Administrator
170 Wood Avenue South
Iselin, NJ 08830

Respectfully submitted,

Peter Lam, Reg. No. 44,855
Attorney(s) for Applicant(s)
Telephone: 650-943-7350
Date: 4/19/05

PAGE 7/8 * RCVD AT 4/19/2005 7:41:48 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:6509684517 * DURATION (mm-ss):02-56